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EXAMINER	
RAHMJOO, MANUCHER	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/632,452	Applicant(s) FORD ET AL.	
	Examiner Mike Rahmjoo	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,9-27 and 31-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-27,31-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 5, 9-21, 23- 27, 31- 45, 53- 56, and 58- 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carlucci et al (US Patent 5,191,645), hereinafter, Carlucci in view of Spannaus et al(US Patent 5,646,651),hereinafter, Spannaus.

As per claims 1, 23, 44, 52 and 57 Carlucci teaches a receiver for receiving a video signal forwarded from a video signal source within the video graphic workstation (the system of figure 1) see for example figure 2 block 70 and figure 3 block 100; a video pipeline for post-processing the received video signal, the video pipeline producing a post-processed video signal see for example figure 2 through block 72 and figure 3 block 102 and configured to perform frame rate matching see for example column 6 lines 25- 37 wherein in order to achieve the desired four fold increase in frame rate each bit written into each one of the buffers has to be read out four times from that buffer; and a video output module for converting the post-processed video signal, the video output module producing a formatted video signal see for example figure 2 through block 74 and figure 3 blocks 104, 106, and 108.

However, Carlucci does not teach the video output system is configured to receive the received video signal from a storage medium, a video graphics processor, and a video input system, wherein the video output system is communicatively coupled to the storage medium, the graphic processor, and the video input system by electrical communication paths.

The examiner broadly interprets Spannaus as teaching the video output system (see for example the output of block 280 in figure 2) is configured to receive the received video signal from a storage medium (see for example figure 2 blocks 240, 220, and 250), a video graphics processor (see for example figure 2 blocks 210, 220, 230, 250 and 260, column 4 lines 41- 60, and column 2 lines 30- 62) and a video input system (see for example figure 2 blocks 200, 210, 220, 230, 240, 250, 260, 270 and 290), wherein the video output system is communicatively coupled to the storage medium, the graphic processor, and the video input system by electrical communication paths see for example the electrical communication paths of figure 2.

It would have been made obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the teachings Spannaus into Carlucci to provide a higher level of integration of video graphics to take advantage of the internal bandwidth of high density memory chips and thus offer a highly versatile, user friendly, technologically advanced and cost effective device see for example column 1 lines 44- 46 and column 4 lines 10- 28.

As per claims 2, 24 and 45 Carlucci teaches an ancillary data injector, the injector inserting ancillary data into the post-processed video signal in figure 2 through block 34 (VTR).

As per claims 3, 4, 25 and 26 Carlucci teaches a generator locking device in figures 8 and 9 through blocks 190 and 180 respectively.

As per claims 5 and 27 Carlucci teaches e-VS is an RGB encoded video signal, an RGBA encoded video signal, a YUV-Type encoded video signal, or a YUVA-Type encoded video signal in column 3 line 48 wherein motion picture film (video) in color or black and white is received by

camera processor 12.

As per claims 9 and 31 Carlucci teaches VS is an analog composite video signal, an analog component video signal, a serial digital composite video signal, a serial digital component video signal, a parallel digital composite video signal, or a parallel digital component video signal in column 7 lines 56- 65 wherein RGB are read out in parallel from buffers to produce three parallel data streams.

As per claims 10 and 32 Carlucci teaches the process of post-processing includes region of interest selection in column 12 lines 32- 38 wherein portion of an image is selected.

As per claims 11 and 33 Carlucci teaches the process of post-processing includes frame rate matching in column 6 lines 25- 37 wherein in order to achieve the desired four fold increase in frame rate each bit written into each one of the buffers has to be read out four times from that buffer.

As per claims 12, 14, 15, 34, 36, and 37 Carlucci teaches the process of picture framing includes letter boxing and the process of spatial adaptation includes spatial adaptation and picture framing in column 12 lines 32- 38 wherein portions of images are selected and occupy distinct portion of the monitor.

As per claims 13 and 35 Carlucci teaches the process of spatial adaptation includes scaling in column 5 lines 54- 60 wherein the resolution is enhanced.

As per claims 16 and 38 Carlucci teaches the process of post-processing includes changing the sample rate of the video signal being post-processed in column 3 lines 54- 60 wherein camera processor generate high definition video signal different than 1.875 fps.

As per claims 17, 18, 39, and 40 Carlucci teaches the process of post-processing includes gamma insertion and removal in column 9 lines 17- 29 wherein gamma correction is made.

As per claims 19 and 41 Carlucci teaches the process of post-processing includes color space

conversion in column 8 lines 40- 52 wherein color transformation of digitized images is made.

As per claims 20 and 42 Carlucci teaches the process of post-processing includes changing frames of video data into interleaved fields of video data in column 5 line 20 through alternating frames stored.

As per claims 21 and 43 Carlucci teaches the process of post-processing includes addressing on a frame-by-frame basis the video signal being post-processed in column 5 line 9.

As per claims 53- 56 and 58- 61 these claims, individually or in combination, are substantially similar to claims 2- 21 and are therefore rejected with the same rational.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carlucci in view of Olarig et al (US Patent 5,937,173), hereinafter, Olarig.

As per claim 22 Carlucci does not teach the system is a Peripheral Component Interconnect circuit board.

However, Olarig teaches the system is a Peripheral Component Interconnect circuit board in column 8 lines 2- 8.

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the teachings of Olarig into Carlucci to make dual use of signal pins on the multiple set core logic chip set which may reduce the number of overall pin count to result into reduction of manufacturing costs in column 8 lines 5- 10.

Claims 46- 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carlucci in view of Spannaus as applied to claim 1 further in view of Kostreski et al (US Patent 5,734,589), hereinafter, Kostreski.

As per claims 46,47,49 and 50 Carlucci and Spannaus do not teach the video output module is a daughter board.

However, Kostreski teaches a daughter board see for example column 9 lines 1- 21 and figure 1.

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the teachings of Kostreski into Carlucci and Spannaus for a technician to replace the module in either the field or the shop so as modify a DET to connect to and communicate over a different network or other implementations further described.

As per claims 48 and 51 Carlucci, Spannaus and Kostreski do not teach the video output informing of its configuration.

However, it is well know in the art to inform of a configuration of any detachable module to the main processor (CPU commonly on the mother board) so as to make and utilize an operational piece of hardware/ software.

Response to Arguments

Applicant's arguments filed 04/08/2004 have been fully considered but they are not persuasive.

Applicant argues on page 18- 19 that Carlucci does not teach or suggest the video output system that is configured to receive a video signal from a storage medium, a video graphics processor, and a video input system wherein the video output system is communicatively coupled to a storage medium, a video graphics processor, and a video input system by electrical communication paths.

In response, the applicant cannot show non- obviousness by attacking references individually whereas here the rejections are based on combination of references. See In re Keller, 208USPTO 871 (CCPA 1981).

As per applicant's remarks on pages 18- 19, applicant argues that Carlucci does not teach applicant's amended claim which recites "the video output system that is configured to receive a video

signal from a storage medium, a video graphics processor, and a video input system wherein the video output system is communicatively coupled to a storage medium, a video graphics processor, and a video input system by electrical communication paths". Applicant further argues on page 20 lines 11- 13 that 1) the signals feeding into the DAC 280 represent already processed signals that are ready for output to a monitor and 2) there would be absolutely no reason to direct these signals to the input processor 70 of Carlucci.

The examiner respectfully disagrees. The signals feeding into the DAC 280 of Spannus are processed **but not ready for output** to a monitor. The processed signals being output through the DAC 280 are ready for output to the monitor. Meanwhile the video signals forwarded from a video signal source to a receiver as well as a signals into the video pipeline for post processing the received video signals are all processed signals. The examiner can not differentiate between the processed signals of the secondary reference of the art and applicant's claimed invention. The second argument raised by applicant to direct these signals to the input processor 70 (page 20 line 12) of Carlucci is null as per rejection made within the office action.

As per applicant's remarks on page 19 lines 19- 24 through page 20 lines 1- 2, the examiner points out to column 4 lines 10- 28 of spannaus which states "The **integration** of Video and Graphics Rasterization along with **associated functional blocks** as described herein, provides a balanced Multi-Media/Graphics **solution to the technology/bandwidth problem** of today's higher density memories. By containing both video, graphic rasterization, and window identifier functionality **on the same chip**, by providing fast Random Access Memory for each, and by sharing and containing the wide bus and high speed accesses to within the chip, a unique and effective solution is thereby provided. The problem is therefore solved in a manner beneficial to both rasterization and video components of Multi-Media and Graphics. The apparatus as described above, includes **the video Interface, Video SRAM, Rasterizer, Pixel SRAM, Frame Buffer, WID functionality, MUX, SAM, Palette, and DACs**. While

the Palette and DACs integration are not essential to this invention, they are desirable in the long run **to minimize the I/Os** on the MGRAM package and **allow lower cost packaging** of the MGRAM module."

As readily seen from the above citation of the prior art, the existence of a single chip module by no means is a deterrent for using Spannaus to overcome the deficiency of Carlucci. On the contrary one can easily see from the above stated paragraph the logic and motivation to incorporate Spannaus into Carlucci. Therefore the MPEP & 2143.01 requirement is established.

Applicant argues on pages 21- 22 that the video pipeline of Carlucci's digital signal processor 72 or Carlucci's A/D converter 102 does not satisfy each of the combination of elements recited in claims 10- 21. The examples used, make a reference to claims 10- 11.

The examiner is **broadly interpreting a receiver, a video pipeline and a video output module** as any I/O device(s) or set(s) of components which reads on applicant's claimed invention. For example refereeing to claim 11 figure 3 depicts a receiver (block 100), a video pipeline (block 70) and a video output (block 102) which performs frame rate matching as per rejection made through claim 11.

As per analogy made through the above paragraph the rejection of claim 22 made in view of Olarig still holds.

In light of the foregoing responses to the arguments and the analogy made, the examiner believes that the arguments per rejections made 1) as per claim 46 on page 23- 24 and in light applicant's admittance of lack of novelty for the use of daughter boards and 2) as per claims 48 and 51 on page 24 (it is noted that in Carlucci for example figure 8 block 190 is a timing unit sync generator used for control of timing signals for informing of its timing in connection with the other CPUs and also for example column 6 lines 53- 63 of Carlucci which shows filter 100 for enhancing the resolution of the input signal and subsequently informing of its configuration) are not valid and therefore the rejections already made still hold.

Applicant argues on page 25 line 14 that the office action is interpreting the claimed video

pipeline as Carlucci's digital signal processor 27.

The examiner points out to the portion of the rejection made which is missing from applicant's remarks which states" a video pipeline for post-processing the received video signal, the video pipeline producing a post-processed video signal see for example figure 2 through block 72 and **figure 3 block 102**". The analogy made above earlier is crucial to understanding examiner's view which states" The examiner is **broadly interpreting a receiver, a video pipeline and a video output module** as **any I/O device(s) or set(s) of components** which reads on applicant's claimed invention.". In light of the foregoing responses as well as the portion cited as missing from applicant's remarks, the examiner's analogy is obviated.

In order to clarify applicant's claimed invention in light of the amendments made examiner respectfully suggests the applicant to incorporate further limitations into the claim language as to read on the applicant's invention and distinguish whether the electrical communication paths are direct or indirect paths.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Rahmjoo whose telephone number is (703) 305- 5658. The examiner can normally be reached on 6:30- 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (703) 308- 6829. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872- 9314 for regular communications and (703) 872- 9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305- 4750.

Mike Rahmjoo

May 10, 2004

Matthew C. Bella

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